A 2.4-GHz Silicon-on-Sapphire CMOS Low-Noise Amplifier

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***Abstract*—A low-noise amplifier operating at 2.4 GHz has been fabricated with MOSFET's in silicon-on-sapphire technology. The amplifier has a 2.8-dB noise figure, 10-dB gain, and 14-dBm output referred IP3 with 14-mW power dissipation. The amplifier was matched for minimum noise with on-chip spiral inductors and capacitors.**

***Index Terms*—Microwave FET amplifiers, noise, MMIC's.**

I. Introduction

IMPROVEMENTS in silicon device performance combined with low cost are making silicon an increasingly attractive technology for microwave wireless communication circuits. One such application is in monolithic transceivers operating in the 1.9–2.4-GHz regime. A key circuit needed for this application is a low-noise amplifier (LNA). There has been much work to date on LNA's, including CMOS LNA's. In [1], Shaeffer gives an excellent summary of CMOS as well as GaAs LNA performance to date. Table I summarizes these recently reported LNA results.

In this letter, we will discuss a CMOS-on-sapphire LNA operating at 2.4 GHz with very good noise figure below 3 dB, which uses on-chip spiral inductor for matching the field-effect transistor (FET) for minimum noise figure. CMOS technology allows integration of both digital and analog circuits on the same chip in order to reduce cost, improve performance, and increase manufacturability by reducing the number of chips and bond wires.

II. Circuit Design and Simulation

The optically defined 0.5-μm gate length metal-reinforced gate n-MOSFET used for this work has been described elsewhere [2], [3]. An aluminum T-gate is used to reduce gate resistance and, hence, lower noise figure and increase $f_{\max}$. The f_t and $f_{\max}$ are 15 and 35 GHz, respectively. The minimum noise figure and associated gain at 2 GHz are 0.9 and 17.5 dB, respectively. The SOS wafer has a 550-μm-thick sapphire substrate with a 1000-Å-thick silicon film improved through ion implantation and solid phase epitaxial regrowth [4]. With the exception of the metal reinforced gate, the process technology is the same as that used for large-scale digital circuits.

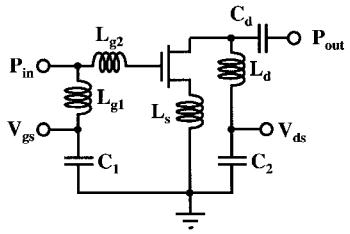

Fig. 1. Circuit schematic of the LNA.

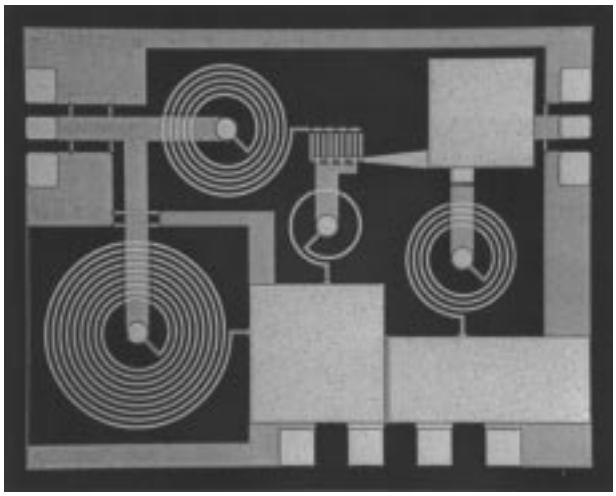

Fig. 2. Photograph of the LNA (Dimensions: 1.3 × 0.95 mm).

Fig. 1 shows the circuit schematic of the single-stage LNA. Spiral inductors [5] are used to match the FET's to the minimum noise figure at $\Gamma_{\rm opt}$. Circuit simulations were carried out using HP/EEsof's LIBRA to determine the optimal gate width of the FET and the value of the matching components. Values of the circuit parameters are given in Table II. For the design, measured two-port S-parameter data was used for the FET's. A gate width of 400 μm (8 μm × 50-μm fingers) was chosen to optimize noise figure and minimize dc power dissipation. Simulations predicted a 2.2-dB noise figure and good matching at 2.4 GHz as shown in Fig. 3.

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TABLE I
SUMMARY OF RECENT CMOS LNA RESULTS

Author	L_g (μm)	Freq. (GHz)	Gain (dB)	NF (dB)	OIP3 (dBm)	-1 dB (dBm)	Power (mW)
This work	0.5	2.4	10	2.8	14	4	14
Chang *et al.* [6]	2	0.75	14	6.0	-	-	7
Karanicolas *et al.* [7]	0.5	0.9	15.6	2.2	12.4	-	20
Sheng *et al.* [8]	1	0.9	11	7.5	-	-	36
Shaeffer *et al.* [1]	0.6	1.5	22	3.5	12.7	0	30

TABLE II
LNA CIRCUIT ELEMENT VALUES

FET		Input			Source	Output		
L_g (μm)	W_g (μm)	L_{g2} (nH)	L_{g1} (nH)	C_1 (pF)	L_s (nH)	L_d (nH)	C_d (pF)	C_2 (pF)
0.5	400	14.8	4.4	40	0.3	2.6	12	60

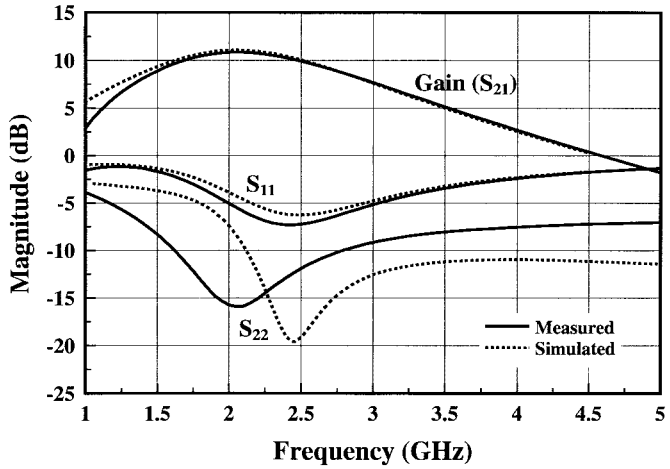

Fig. 3. Gain and matching of the LNA versus frequency.

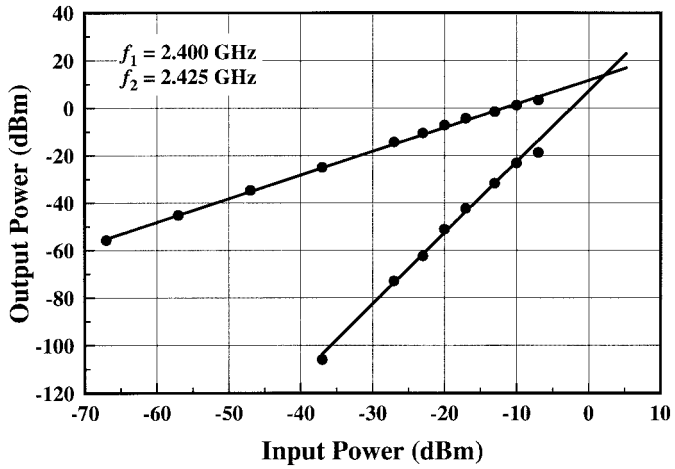

Fig. 4. Two-tone linearity characteristics of the LNA.

The circuit was laid out for on-wafer probing with 100-μm pitch coplanar ground-signal-ground microwave probes output and includes on-chip bias tees for the gate and drain biases. A photograph of the fabricated switch is shown in Fig. 2. Dimensions of the chip are 1.3 mm $\times$ 0.95 mm.

III. MEASUREMENTS

The LNA was operated at $V_{\rm ds} = 1.5$, $V_{\rm gs} = 0.7$ V. The dc current consumption at low input power levels is 8.8 mA (while it rises to 9.9 mA for an input power corresponding to the 1-dB compression point). This corresponds to an average power dissipation of 14 mW. The gain (S_{21}) and matching (S_{11}, S_{22}) of the amplifier versus frequency (from 1 to 5 GHz) are shown in Fig. 3. Using the spiral inductors, the LNA is well matched for gain at 2.4 GHz as observed by S_{11} and S_{22} values below -7 dB. With the exception of the output matching, the measured data agreed well with the simulations. Two-tone ($f_1 = 2.4$ GHz, $f_2 = 2.425$ GHz) linearity measurements of the LNA were done and the results are plotted in Fig. 4. The output referred 1-dB compression point and third-order intercept (OIP3) are 4 and 14 dBm, respectively. Noise measurements performed with an HP8970A Noise figure meter yielded a 2.8-dB noise figure at 2.4 GHz.

IV. DISCUSSION OF RESULTS

These results represent the highest frequency CMOS low noise amplifier reported to date. As seen in Table I, our LNA has one of the lowest noise figure and power dissipation reported and operates at roughly twice the frequency. The noise characteristics of this LNA are of the order of those required for numerous wireless systems and on the same order as obtained with silicon bipolar circuits. The improved microwave characteristics are as expected by the lower parasitic substrate and the higher conductivity gate metallization. On the basis of simulation, we believe that even lower noise figure would be possible if the metal thickness used to realize the on-chip inductors was greater. The ratio of OIP3 to the dc power consumption is 1.2. The excellent linearity observed may be attributed to the good turn-off and low output conductance of the SOS FET's, together with the absence of the body effect. The combination of low noise figure, high OIP3, and low power consumption is particularly desirable for wireless receiver circuits.

V. Conclusion

A low-noise amplifier operating at 2.4 GHz has been fabricated in silicon-on-sapphire MOSFET technology. The LNA has a 2.8-dB noise figure with 10-dB associated gain with 14-mW power dissipation. The output referred 1-dB compression point and third-order intercept point are 4 and 14 dBm, respectively. With the exception of the metal-reinforced gate to reduce gate resistance, the amplifier utilizes the same technology used for large-scale digital CMOS circuits. Hence, the LNA is well suited for low power transceiver on a chip circuits incorporating both radio frequency and digital CMOS circuits on the same substrate.

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